

Application No.: 09/786,524
Amendment Dated: July 27, 2005
Reply to Office Action of: April 27, 2005

MAT-8097US

Amendments to the Drawings:

The attached sheet of drawing includes changes to Figure 15. This sheet replaces the original sheet.

Remarks/Arguments:

In the Drawings, the element "1050" has been correctly labeled "1505" in Figure 15.

Claims 1-11 are pending. Claims 1-11 have been amended. No new matter has been introduced herein.

Claims 1-3 and 8 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Taniguchi et al. (EP 0917145 A2) in view of Takeshita et al. (U.S. Patent No. 5,179,451). It is respectfully submitted, however, that these claims are now patentable over the cited art for the reasons set forth below.

Claim 1, as amended, includes features neither disclosed nor suggested by the cited art, namely:

... transmitting means for transmitting n frames of transmission data in parallel by restructuring the data of n frames into a main data output and a sub data output on the basis of said data information ...

These features are disclosed, for example, p. 4, line 24 - p.12, line 25, and Figure 1.

Taniguchi et al. disclose signal reproduction method for slow reproduction. Taniguchi et al. disclose a memory 109 to stores n frames of data while a first-in-first-out (FIFO) memory 110 stores data delayed by one field. A switch 111 selects between data 109 and delayed data 110 (p. 4, paragraphs 27-28). Taniguchi et al. do not disclose or suggest Applicants' claimed feature of "... transmitting means for transmitting n frames of transmission data in parallel by restructuring the data of n frames into a main data output and a sub data output on the basis of said data information..." (emphasis added). These features are neither disclosed nor suggested by Taniguchi et al. Thus, Taniguchi et al. do not include all of the features of amended claim 1.

Takeshita et al. disclose a signal reproduction method for slow reproduction. Takeshita et al. disclose that a video signal is made up of blocks having an ID signal

which indicates the field number and frame number. Blocks rid of error are stored in address locations corresponding to ID signals in the memory (Col, 1, lines 26-35). However, Takeshita et al. do not make up for the features that are lacking in Taniguchi et al., namely, "... transmitting n frames of transmission data in parallel by restructuring the data of n frames into a main data output and a sub data output." Accordingly, allowance of claim 1 is respectfully requested.

Claims 2 and 3 include all of the features of claim 1 from which they depend. Accordingly, claims 2 and 3 are also patentable over the art of record.

Claim 8, as amended, includes features neither disclosed nor suggested by the cited art, namely:

... delay means for issuing n frames of data read out by said memory reading means by delaying one parallel output of said memory reading means by each of one field and two fields, and delaying a second parallel output by each of one field, two fields and three fields ...

These features are disclosed, for example, p. 13, line 17 - p. 14, line 5, and Figure 9.

Taniguchi et al. disclose a FIFO memory 110 to delay data by one field and a switch 111 for selecting between data stored in memory 108 and data delayed by one field in FIFO memory 110. Taniguchi et al do not disclose or suggest Applicants' claimed features of "... delay means for issuing n frames of data ... by delaying one parallel output of said memory reading means by each of one field and two fields, and delaying a second parallel output by each of one field, two fields and three fields" (emphasis added). Applicants' amended claim 8 thus includes delay means that provides multiple outputs based on receiving parallel inputs of data from the memory reading means. These features are neither disclosed nor suggested by Taniguchi et al. Thus, Taniguchi et al. do not include all of the features of amended claim 8.

Takeshita et al. is described above. Takeshita et al. do not make up for the features that are lacking in Taniguchi et al., namely, "... delay means for issuing n frames of data ... by delaying one parallel output of said memory reading means by

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each of one field and two fields, and delaying a second parallel output by each of one field, two fields and three fields." Accordingly, allowance of claim 8 is respectfully requested.

Claims 5, 6 and 9 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Taniguchi et al. in view of Takeshita et al. and Mitsuta et al. (JP 09-069261). Claims 5 and 6 include all of the features of claim 1 from which they depends. Mitsuta et al. do not make up for the features that are lacking in Taniguchi et al. and Takeshita et al. Accordingly, claims 5 and 6 are also patentable over the cited art.

The rejection of claim 9 is respectfully traversed. Neither Taniguchi et al., Takeshita et al. nor Mitsuta et al. disclose or suggest Applicants' features of:

... second memory means for accumulating the data of n frames read out by said memory reading means for the portion of three frames ...

... reproduction output control means for selecting and issuing field data on the basis of the data information, from the data delayed by one frame and two frames by controlling said second memory means ...

Taniguchi et al. is discussed above. Taniguchi et al. do not disclose or suggest Applicants' features of "... second memory means for accumulating the data of n frames read out by said memory reading means for the portion of three frames ... reproduction output control means for selecting and issuing field data on the basis of the data information, from the data delayed by one frame and two frames by controlling said second memory means..." (emphasis added). These features are neither disclosed nor suggested by Taniguchi et al. Thus, Taniguchi et al. do not include all of the features of claim 9.

Takeshita et al. is discussed above. Takeshita et al. do not disclose or suggest Applicants' features of "... second memory means for accumulating the data of n frames read out by said memory reading means for the portion of three frames ... reproduction output control means for selecting and issuing field data on the basis of the data information, from the data delayed by one frame and two frames by

controlling said second memory means ..." (emphasis added). These features are neither disclosed nor suggested by Takeshita et al. Thus, Takeshita et al. do not include all of the features of claim 9.

Mitsuta et al. discloses a reproducing apparatus which sends a reproduction signal from a magnetic tape to three memories arranged in parallel. A write memory selection switch and a read memory selection switch are controlled so that writing and reading of data are not carried out at the same memory. (Abstract, lines 7-13) Mitsuta et al., however, does not make up for the features that are lacking in Taniguchi et al. and Takeshita. Namely, "...second memory means for accumulating the data of n frames read out by said memory reading means for the portion of three frames ... reproduction output control means for selecting and issuing field data on the basis of the data information, from the data delayed by one frame and two frames by controlling said second memory means ..." (emphasis added). Accordingly, allowance of claim 9 is respectfully requested.

Claims 4 and 10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Taniguchi et al. in view of Takeshita et al., further in view of Saito et al. (U.S. Patent No. 5,838,249). These claims, however, also include all of the features of claim 1 from which they depend. Saito et al. do not make up for the features that are lacking in Taniguchi et al. and Takeshita et al. Accordingly, claims 4 and 10 are also patentable over the cited art.

Claims 7 and 11 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Taniguchi et al. in view of Takeshita et al. and Mitsuta et al., further in view of Saito et al. These claims, however, also include all of the features of claim 1 from which they depend. Mitsuta et al. and Saito et al. do not make up for the features that are lacking in Taniguchi et al. and Takeshita et al. Accordingly, claims 7 and 11 are also patentable over the cited art.

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In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,


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DG/fp

Attachment: Figure 15 (1 sheet)

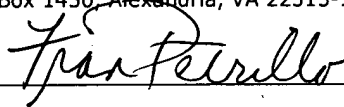
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